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# TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
**ITL.0700US**

In Re Application Of: **Lei Cheng**

| Application No. | Filing Date | Examiner | Customer No. | Group Art Unit | Confirmation No. |
|---|---|---|---|---|---|
| 10/082,893 | February 26, 2002 | Kim T. Huynh | 21906 | 2112 | 2799 |

Invention: **Directly Transferring Transmit Data in an Embedded Adapter**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **February 7, 2006**

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Dated: **April 7, 2006**

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**Nancy Meshkoff**

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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | Lei Cheng | Art Unit: | 2112 |
| Serial No.: | 10/082,893 | Examiner: | Kim T. Huynh |
| Filed: | February 26, 2002 | Atty Docket: | ITL.0700US (P13936) |
| For: | Directly Transferring Transmit Data in an Embedded Adapter | Assignee: | Intel Corporation |

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# APPEAL BRIEF



Date of Deposit: April 7, 2006
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Nancy Meshkoff

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## REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

## RELATED APPEALS AND INTERFERENCES

None.

## STATUS OF CLAIMS

Claims 1-30 (Rejected).

Claims 1-30 are rejected and are the subject of this Appeal Brief.

## STATUS OF AMENDMENTS

All amendments have been entered.

## SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1, for example, calls for transferring data from a host memory to an Ethernet device. The data is processed without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device. Thus, to simplify, an adapter includes an Ethernet device and the adapter also includes an embedded memory. Data may be transferred from the host memory to the Ethernet device without sending the data to the embedded memory associated with the adapter.

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:

transferring data from a host memory to an Ethernet device (Figure 5, elements 110-116); and

processing the data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device (Figure 5, elements 110-116) (specification at page 6, line 26 to page7, line 2; page 7, lines 17-22).

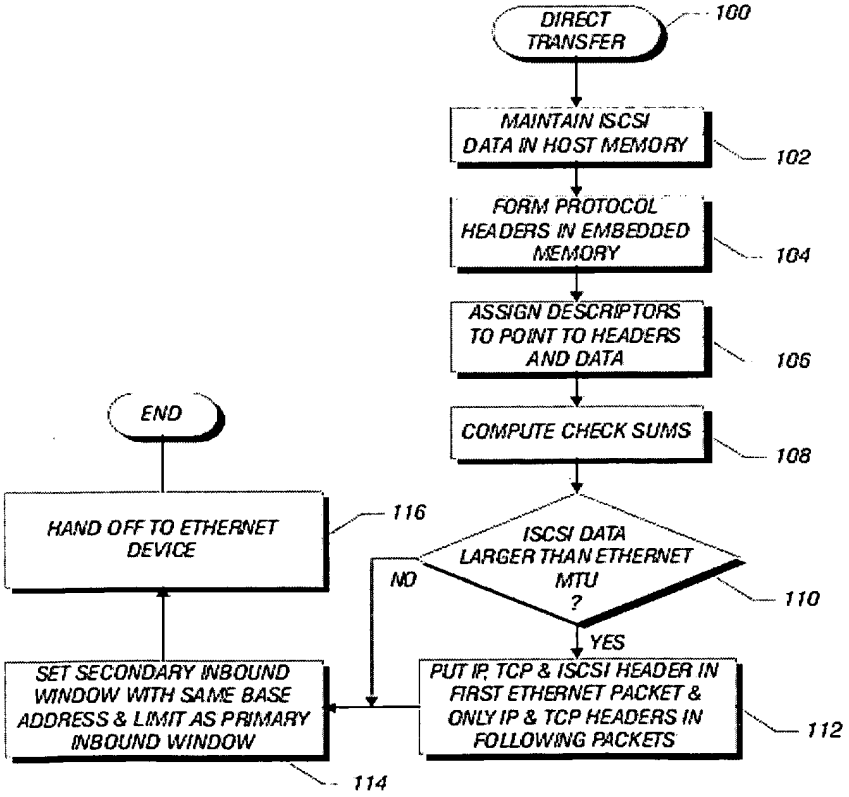


FIG. 5

11. An article comprising a medium storing instructions that enable a processor-based system to:

transfer data from a host memory to an Ethernet device (Figure 5, elements 110-116); and

process the data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device (Figure 5, elements 110-116) (specification at page 6, line 26 to page7, line 2; page 7, lines 17-22).

21. An adapter comprising:

a processor (Figure 1, 34) to communicate with a host system (Figure 1, 14) including a host memory (18) (specification at page 3, lines 16-20);

an Ethernet device (Figure 1, 30) coupled to said processor (Figure 1, 34) (specification at page 3, lines 16-20); and

an embedded memory (Figure 1, 32) coupled to the processor (Figure 1, 34) to enable data to be transferred directly from the host memory (18) to the Ethernet device (30) without being copied to said embedded memory (Figure 1, 32) (specification at page 3, line 21 to page 4, line 4).

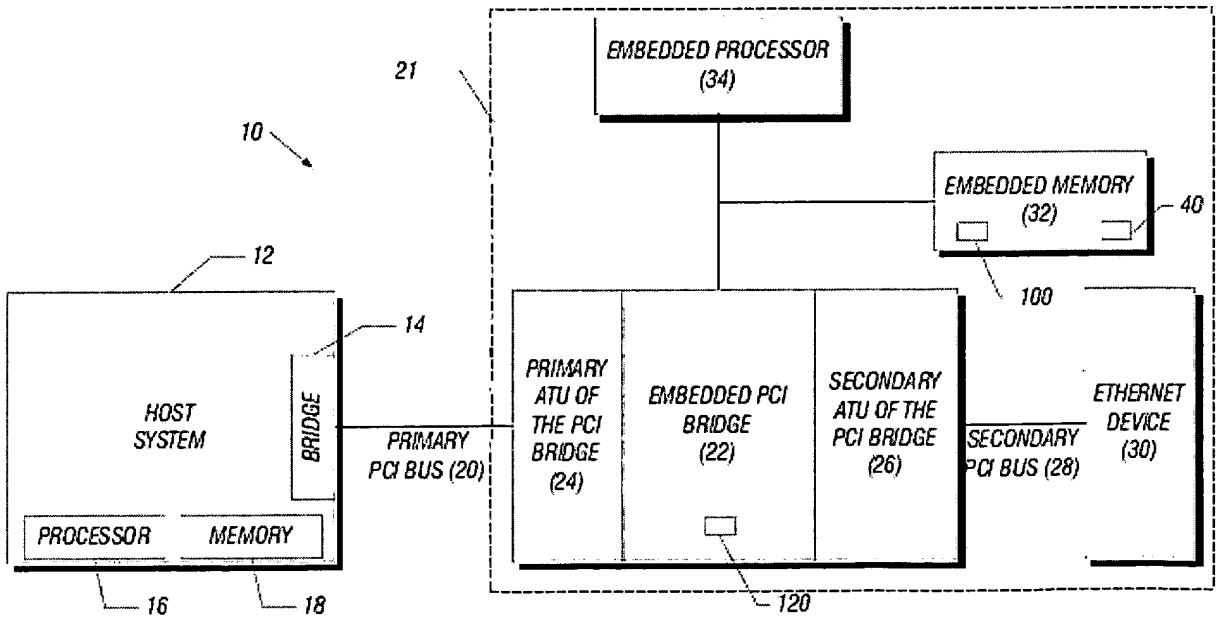


FIG. 1

26. A system comprising:

a host processor (16, Figure 1) (specification at page 3, lines 5-7);

a host memory (18, Figure 1) coupled to said host processor (16, Figure 1) (specification at page 3, lines 5-7);

a bridge (14, Figure 1) coupled to said host processor (specification at page 3, lines 5-7); and

an adapter (21) coupled to said bridge (14), said adapter including a processor (34), an embedded memory (32) and an Ethernet device (30), said adapter (21) to transfer data directly from said host memory (18) to said Ethernet device (30) without copying the data to the embedded memory (32) (specification at page 3, line 4 to page 4, line 4).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

**A. Are claims 1-30 anticipated by Davis?**

## ARGUMENT

### A. Are claims 1-30 anticipated by Davis?

Claim 1, for example, calls for transferring data from a host memory to an Ethernet device. The data is processed without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device. Thus, to simplify, an adapter includes an Ethernet device and the adapter also includes an embedded memory. Data may be transferred from the host memory to the Ethernet device without sending the data to the embedded memory associated with the adapter.

Conventionally, data is copied to the embedded memory from the host, the Ethernet packet is formed, and the packet is put in the transmit buffer in the embedded memory. This operation involves making one copy of data from the host to the embedded memory. This copy decreases the performance of the adapter. See the specification at page 1, line 20 through page 2, line 2.

It is respectfully submitted that not a single limitation of any independent claim is taught by the cited reference. Under the following headings, the various limitations are discussed and the failure of the reference to teach a single one of the claimed elements is pointed out. Therefore, the rejection should be reversed.

#### 1. Transferring Data from a Host Memory

There is no discussion of any transferring data from a host memory in the reference. Instead, what is happening and what is relied on in the office action is a configuration cycle wherein peripheral devices are identified. However, no data is transferred to them. The assertion that the drivers are loaded into the peripheral devices is an incorrect understanding of how computers operate. Drivers are never loaded into peripheral devices. Nothing in the reference ever suggests anything of the sort.

The argument that sending configuration commands to the I/O processor or anything else is some kind of providing of data is simply baseless. Nothing in any of the material supports this.

2. Ethernet Device

There is absolutely no mention in the reference of any Ethernet device. Therefore, there cannot be transferring of anything to an Ethernet device. The Examiner suggests that an Ethernet device is never claimed, but, in fact, it is clearly the object of the acts set forth in the first element of claim 1.

Therefore, there is not a *prima facie* rejection since there is no Ethernet device in the cited reference.

3. Processing Data without Sending the Data from the Host Memory to an Embedded Memory Associated with an Adapter that Includes the Ethernet Device

There is no teaching in the reference of how, if there were an Ethernet device and how if data was transferred to the Ethernet device, that data could be transferred without transferring it to an internal memory of the Ethernet device. Since there is discussion of an Ethernet device and no discussion of how it operates, it is impossible for the cited reference to anticipate.

While the Examiner argues that there is no requirement of an embedded memory of an Ethernet device, there is a requirement that data be transferred without implicating that embedded memory. This requires that there be some transfer to a device that is an Ethernet device and that there be some way to accomplish that transfer without using an embedded memory. Since there is no Ethernet device, and there is no inclination to transfer data to an Ethernet device, the reference is completely and totally irrelevant. The suggestion that any PCI device is equivalent to an Ethernet device or to accessing and providing data to that Ethernet device without using the embedded memory is baseless.

Therefore, the rejection should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: April 7, 2006

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## CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:

transferring data from a host memory to an Ethernet device; and

processing the data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device.

2. The method of claim 1 including forming protocol headers in the embedded memory.

3. The method of claim 1 including assigning descriptors to point to headers and data.

4. The method of claim 3 including assigning descriptors to point to headers and data in said embedded memory and host memory.

5. The method of claim 1 including computing checksums in firmware and in the Ethernet device.

6. The method of claim 1 including determining whether data in said host memory is larger than an Ethernet maximum transmit unit.

7. The method of claim 6 wherein if said data is larger than an Ethernet maximum transmit unit, placing said data in at least two different Ethernet packets.

8. The method of claim 7 including placing more headers in one Ethernet packet than in another Ethernet packet.

9. The method of claim 1 including forming a primary inbound window to receive data from a host and forming a secondary inbound window to receive data from said Ethernet device, said secondary inbound window having the same base address and limit as the primary inbound window.

10. The method of claim 1 including detecting the address of an access request from an Ethernet device and routing said request to the host memory or embedded memory based on the address.

11. An article comprising a medium storing instructions that enable a processor-based system to:

transfer data from a host memory to an Ethernet device; and

process the data without sending the data from the host memory to an embedded memory associated with an adapter that includes the Ethernet device.

12. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to form protocol headers in the embedded memory.

13. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to assign descriptors to point to headers and data.

14. The article of claim 13 comprising a medium storing instructions that enable a processor-based system to assign descriptors to point to headers and data in both said embedded memory and host memory.

15. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to compute checksums in firmware and in the Ethernet device.

16. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to determine whether data in said host memory is larger than an Ethernet maximum transmit unit.

17. The article of claim 16 comprising a medium storing instructions that enable a processor-based system to, place said data in at least two different Ethernet packets if said data is larger than an Ethernet maximum transmit unit.

18. The article of claim 17 comprising a medium storing instructions that enable a processor-based system to place more headers in an Ethernet packet than in another Ethernet packet.

19. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to form a primary inbound window to receive data from a host and form a secondary inbound window to receive data from said Ethernet device, said secondary inbound window having the same base address and limit as the primary inbound window.

20. The article of claim 11 comprising a medium storing instructions that enable a processor-based system to detect the address of an access request from an Ethernet device and route said request to the host memory or embedded memory based on the address.

21. An adapter comprising:

a processor to communicate with a host system including a host memory;

an Ethernet device coupled to said processor; and

an embedded memory coupled to the processor to enable data to be transferred directly from the host memory to the Ethernet device without being copied to said embedded memory.

22. The adapter of claim 21 including descriptors that point to headers and data in said host memory and said embedded memory.

23. The adapter of claim 21 wherein said processor determines whether data in the host memory is larger than an Ethernet maximum transmit circuit.

24. The adapter of claim 23 wherein said processor places said data in at least two different Ethernet packets when said data is larger than said maximum transmit circuit.

25. The adapter of claim 24 wherein said processor places more headers in one Ethernet packet than in another Ethernet packet.

26. A system comprising:

a host processor;

a host memory coupled to said host processor;

a bridge coupled to said host processor; and

an adapter coupled to said bridge, said adapter including a processor, an embedded memory and an Ethernet device, said adapter to transfer data directly from said host memory to said Ethernet device without copying the data to the embedded memory.

27. The system of claim 26 wherein said bridge detects the address of an access request from said Ethernet device and routes said request to the host memory or embedded memory based on said address.

28. The system of claim 26 wherein said bridge includes a primary and secondary address translation unit, a primary memory coupled to the primary address translation unit and a secondary memory coupled to the secondary address translation unit.

29. The system of claim 28 wherein the primary inbound window of said primary memory is of the same size as the secondary inbound window of said secondary memory.

30. The system of claim 29 wherein said embedded memory is cacheable.

## EVIDENCE APPENDIX

None.

## RELATED PROCEEDINGS APPENDIX

None.